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Impact of Dimensional Scaling and Size Effects on Beyond CMOS All-Spin Logic Interconnects

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Abstract

The energy-per-bit and delay of All-Spin Logic (ASL) interconnects have been modeled. Both Al and Cu interconnect channels have been considered and the impact of size effects and dimensional scaling on their potential performance has been quantified. It is predicted that size effects will affect ASL interconnects more severely than electrical interconnects.

I. Introduction

As Si CMOS technology approaches its scaling limits, there is a global search for novel devices based on state variables other than electronic charge. Among the potential alternative state variables, electron spin has received special attentions thanks to its advantages in terms of robustness, non-volatility, and enhanced functionality [1]. Research on memory related applications of spin accelerated the science and engineering of manipulating electron spin. Recently, all-spin logic (ASL) has been proposed as a potential beyond CMOS device/interconnect technology [15]. In an ASL device, binary information is stored in the magnetization of magnets that communicate using spin currents. These pure spin currents can be detected at the receiver magnet through the spin-torque effect.

Various materials are suggested to be used to implement the channel in ASL such as metals (Cu and Al), semi-conductors (Si and GaAs), and even novel carbon-based material such as grapheme [2]. Metals have a great advantage due to their high conductivity which helps to reduce the "conductivity mismatch" problem prevalent in spin devices with both semiconducting and graphene channels [9]. However, the spin relaxation length in metals is generally short (<1μm) and gets even shorter if there are excessive scattering at the surfaces or grain boundaries at nano-scale dimensions [2].

In this paper, the energy and delay of metallic ASL interconnects are quantified as functions of interconnect width and length. It is shown that size effects, i.e. surface and grain boundary scattering, will have a significant impact on the potential performance of the ASL interconnects and interconnects continue to be an ever growing concern even for this beyond CMOS technology. However, interconnect capacitance plays no role in the energy dissipation or speed of ASL interconnects. Thereby, there will be no need for ultra-low k dielectric materials, which all pose major process and integration challenges due to their poor mechanical and thermal properties.

II. Interconnect Operation

The basic interconnect element in a metallic ASL is the non-local spin valve (NLSV) structure shown in Fig. 1. An electrical current flows from the power supply to ground through the input ferromagnet (FM) and the nonmagnetic metal underneath it. Electrical current passing through a FM becomes spin polarized with majority electrons' magnetic moment aligned with its magnetization. The spin polarized electrons injected (or extracted) by the input magnet increase (or decrease) the density of the electrons with the spin orientation aligned with the input FM inside the interconnect. The concentration gradients for electrons with parallel and anti-parallel spin orientations inside the interconnect creates a spin current towards the output magnet based on the diffusion process. This spin current applies a torque to the output magnet that, if strong enough, can flip it to align it with the spin orientation of the majority electrons.

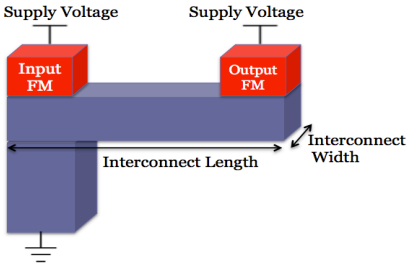

Fig. 1: NLSV interconnects consists of two FMs connected by a non-magnetic channel. Injected spin current from Input FM to the channel diffuses along the interconnect and applies a torque to the output FM

Major parameters that determine the performance and energy dissipation of this interconnect include interconnect and interface resistances, metal diffusion coefficient, spin diffusion length, and the energy potential barrier for the output magnet. In this interconnect, voltage is not being switched and there is no CV^2 energy dissipation. Instead, energy is dissipated only in the form of joule heating in the electrical current path. Therefore, small resistances are desired. Signal transport delay is determined by diffusion coefficient and length. However, the transport delay is considerably smaller compared to the magnet switching time. Magnet switching time depends on the spin current entering the output magnet and the size and properties of the magnet. The spin current at the output depends on the initial spin current and the loss along the length of the interconnect. Signal loss increases exponentially as the ratio of the interconnect length to spin relaxation length increases. Since the magnet flip time is a strong function of the spin current at the end of the interconnect, an increase in loss, either due to a longer interconnect or a shorter spin relaxation length, results in higher delays and energy per bit.

III. Size Effects

Size effects caused by extra scattering at surface and grain boundaries affect several important parameters for ASL interconnects including resistivity, diffusion coefficient, and spin relaxation length. Among these factors, spin relaxation length is the most important factor since signal attenuates exponentially as interconnect becomes longer than spin relaxation length. In metals, the dominant spin relaxation mechanism is the Elliott-Yafet (EY) mechanism in which every time an electron is scattered, there is a certain probability that it may lose its spin information [17]. Hence, spin relaxation time is proportional to momentum relaxation time, which gets shorter as interconnect cross-sectional dimensions become smaller, due to size effects. The models for spin relaxation time and spin diffusion length are presented in [2] and Fig. 2 shows how spin relaxation length decreases as interconnect dimensions scale.

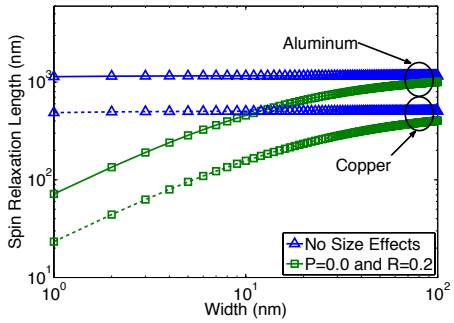

Fig. 2: Spin Relaxation versus Interconnect Width [2]. Size effects cause the spin relaxation length to decrease with decreasing channel width. For the no size effect case, spin relaxation length is independent of Interconnect width

The three important parameters of concern for the purposes of this paper are the sidewall specularity, P, the grain boundary reflectivity, R, and the average grain size. As a rule of thumb, the average grain size in interconnects fabricated by Dual Damascene process is equal to the width or thickness, whichever is smaller [16].

IV. Circuit Models

To model an ASL interconnect, one needs to account for the magnet dynamic, electronic and spintronic transport through magnet to non-magnet interfaces, electric currents, and spin diffusion. Magnet orientation and electron spin are both vectors and therefore need to be represented in terms of their x, y, and z components. A comprehensive equivalent circuit model that captures all these effects has been developed in [3]. The magnetic orientations of the input and output magnets, are modeled by a set of capacitors and voltage-dependent current sources. Two sets of current sources model the interfaces between the interconnect to input and output magnets. The electrical voltage and current and the x, y, and z components of spin density along the interconnect are modeled by four different distributed RC paths, one for electrical voltage and current and three for x, y, and z components of spin density. The effect of thermal noise in magnets is quite important and is accounted for by using white noise voltage signal sources in the two magnets models. The length, width, and height of the magnets are assumed to be 75.6 nm, 37.8 nm, and 3 nm, respectively [4][5]. Following magnets parameters are assumed: α=0.0021, γ =17.60 × 10^{10} 1/sT, M_S =2.5 × 10^5 A/m, $K_{Anisotropy}$=6.0 × 10^4 J/m^2 [4][5].

IV. Simulation Results

The delay and energy per bit have been plotted versus length in Figs. 3 and 4, respectively, assuming a supply voltage of 0.08V, an interconnect width of 37.8 nm equal to the width of the nanomagnets, and a width to thickness aspect ratio of 2. To observe the impact of size effects, a hypothetical case in which size effects are absent is also considered (labeled ideal Cu). Size effect parameters are assumed to be R=0.2, P=0.0 for the typical case, and R=0, P=1.0 are assumed for the ideal case. Physical parameters of Cu interconnect are calculated as σ=41.549 $(\mu\Omega m)^{-1}$, D=0.014 m/s for the typical case. To demonstrate the effect of thermal noise in magnets, each simulation is repeated three times considering room temperature.

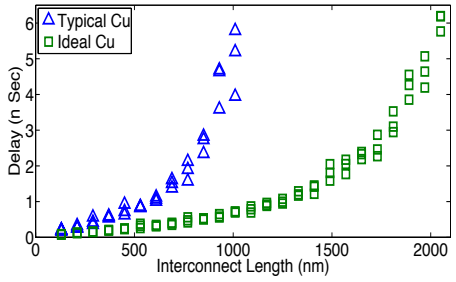

Fig.3: Delay dependency on interconnects length, interconnect width = 37.8 nm, interconnect height= 18.9 nm

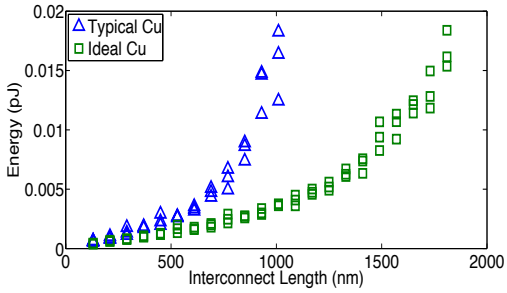

Fig. 4: Energy per bit versus interconnects length (L_{int}). Dimensions are the same as those in Fig. 3

It can be seen that size effects increase the delay and energy dissipation of ASL interconnects significantly if interconnects are longer than a few hundred nanometers. For instance, for a 1μm long interconnect, size effects increase delay and energy per bit by 9 and 5 times, respectively. Also, the exponential increase in delay and energy as interconnect length increases highlights the need for using these interconnects only for short local interconnects. For longer interconnects, spin signals must be converted to electrical signals.

To see how improving interconnect process can improve interconnect performance and energy dissipation, Figs. 5 and 6 plot delay versus surface specularity parameter, P, and grain boundary scattering, R. Both Cu and Al have been considered here. Also, to avoid busy plots, thermal noise has been turned off and its effect has been considered only in setting the initial angles of the magnets [3]. Here, both Cu and Al have been considered as they offer different trade offs. As Fig. 2 shows, spin relaxation in Al is higher than that of Cu. Also, since the mean free path in Al is shorter than that of Cu, size effects are less severe in Al as compared to

Cu. However, Cu offers a lower resistivity unless cross-sectional dimensions become too small such that size effects become too prominent. The spin injection coefficients for Co/Cu and Co/Al interfaces are assumed to be the same [3].

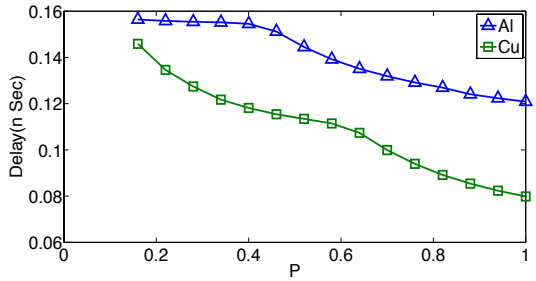

Fig. 5: Delay versus specularity parameter, *P*, for an 80nm long interconnect. Grain boundary scattering parameter, *R*, is assumed to be 0.2 [10-13]

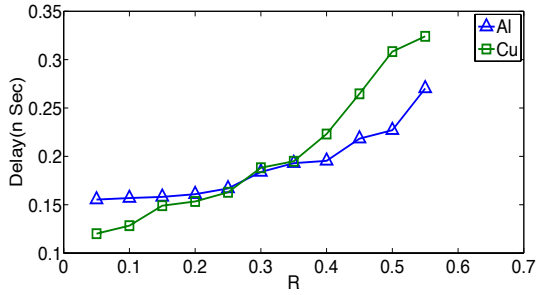

Fig. 6: Delay versus grain boundary reflection probability for an 80nm long interconnect. The specularity parameter, *P*, is assumed to be 0 [10-13]

To quantify the impact of dimensional scaling, interconnect width analysis is presented in Figs. 7 and 8. The FM width is assumed to be 37.8 nm in all cases to ensure adequate magnet stability and non-volatility. Size effects become more pronounced at smaller dimensions. The aspect ratio of interconnect is assumed to be constant in these simulations. For the interconnect widths smaller than the FM width, the interface area decreases which further increases delay and energy.

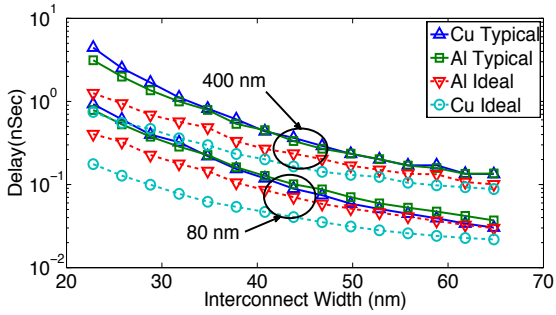

Fig.7: Delay versus interconnect width for 80nm and 400nm long interconnects

For interconnect width analysis, two interconnect lengths of 80nm and 400nm have been considered. For the ideal cases (no size effects), both lengths are shorter than spin relaxation lengths in Cu and Al, and Cu is a better choice since it offers a lower resistivity. However, size effects make the spin relaxation length shorter and Al interconnects become faster and dissipate less energy compared to Cu interconnects especially at small widths. Also, one can see the delay and energy penalty associated with size effects increase drastically as wire dimensions scale down.

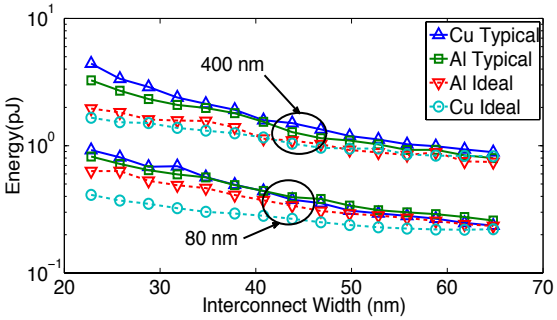

Fig. 8: Energy per bit versus interconnect width for 80nm and 400nm long interconnects

V. Conclusion

Beyond CMOS devices are being studied to potentially augment conventional CMOS logic. Spintronic devices are potential candidates as the offer new features such as non-volatility. In this paper, the potential performance of All-Spin Logic (ASL) interconnects has been modeled and the impact of size effects and dimensional scaling are quantified. It is predicted that ASL interconnects will suffer from size effects even more seriously as compared to their electrical counterparts. This is due to the exponential drop in spin signal as spin relaxation length degrades due to size effects. Thereby, any improvement in Cu interconnect technology such as an increase in average grain size or wire surface quality will have an even bigger impact on ASL interconnects. Al wires offer a larger spin relaxation length and less pronounced size effects as compared to Cu wires. However, they are more resistive except for narrow wires. Thereby, Al ASL interconnects outperform Cu ASL interconnects when are they are relatively long and narrow.

Acknowledgement

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